ABSTRACT

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The present invention provides a clock signal input circuit that is able to provide inverse internal clock signals generated by the same input buffer as the address and data signals which exhibit reduced skew. When a skewed external noninverse clock signal and a corresponding external inverse clock signal are passed through respective reference voltage input buffers there is no reduction in skew between the two internal signals. In a preferred embodiment, the invention provides back to back inverters connected to both lines carrying the noninverted and inverted internal clock signals. The slower internal clock signal has an extra inverter driving it when it switches states and the faster internal clock signal has an extra inverter fighting it when it switches states. The skew of the two signals is reduced, allowing for faster operation of the integrated circuit and a reduction in misread data signals.